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Applications Specific Integrated Circuits

The current trend in electronics systems is towards systems that are more complex, faster and smaller than those available in earlier generations. This has become feasible due to the availability of custom components or Applications Specific Integrated Circuits (ASICs). DRDO has been gearing up to meet the challenges posed by this shift in the design philosophy since the creation of a CORE Group for VLSI Design in 1993.

Several ASICs as well as generic chips have been developed to meet the requirements of various DRDO projects and programmes. Some of the devices developed are described here. Though many of these devices have been developed for specific projects, the devices are generic enough to be used in other applications.

☐ **Pythagora's Processor**

This ASIC converts cartesian coordinates to polar coordinates. The chip accepts 16-bit real (x) and 16-bit imaginary (y) inputs. The inputs can be given as 2s complement or sign magnitude formats. The polar coordinates are computed using the CORDIC algorithm, with 23 stages of pipelining. The cordic algorithm is implemented using adders/subtractors and a multiplier. The magnitude output can be scaled in amplitude by factors of 2, 4 or 8.

Features

- * 16-bit real and imaginary inputs
- * 16-bit magnitude output and 12-bit phase output
- * 20 MHz operation

The Pythagora's processor can compute the magnitude and phase of the vector. This operation finds a variety of applications in digital signal processing. One such application is in digital moving target indicator (MTI).

☐ **Frequency Synthesizer**



This chip was designed to meet the requirements of SONAR systems. The device works on the principle of direct digital frequency

synthesis. It takes the user set values of frequency and phase as inputs. These inputs are given as digital code words and the output is obtained as digital values for sine/cosine waveforms. The user must connect a digital-to-analog converter (DAC) externally to obtain an analog output.

Specifications	
Frequency resolution	0.024 Hz
Operating frequency	25 MHz
Max output frequency	48.8 KHz (8 Samples @ 25 MHz)
No. of channels	3 to 64
External interface	8 bits

□ ANUCO

ANUCO is a floating point arithmetic Coprocessor. It supports floating point addition, subtraction, multiplication, division and format conversions. It is a memory-mapped peripheral and can be used with any general purpose microprocessor to obtain enhanced floating point performance. The device supports only the basic arithmetic operations. Other functions such as transcendental functions, trigonometric functions etc. are supported through a run-time library.

ANUCO has been designed to implement all the arithmetic functions in hardware. The chip has an instruction repertoire of 46 instructions. These include data movement, format conversions, arithmetic operations etc. The design uses a pipelined architecture to provide floating point addition and multiplication.



ANUCO has been successfully interfaced with MC68030, i80386 and i80286 based systems. The device is three to ten times faster than the standard floating point processors available commercially for these processors.

Applications Specific Integrated Circuits - Chip Details				
ASIC Chip	Parameters			
	Die Size (sq. mm)	Parameters Complexity (gates)	Package (pin CPGA)	Technology
Pythagora's Processor	72	18000	84	1 micron std.cell
Frequency Synthesizer	32	10000	68	1 micron std.cell
ANUCO	196	43000	208	0.8 micron Gate Array
MMAC	92	20000	144	1 micron std.cell
FMAC	36	12000	120	1 micron std.cell
Inverse Pythagora's	78	28000	84	1 micron

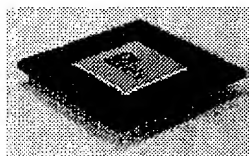
Processor				std.cell
CMUL	68	18000	140	1 micron std.cell
ANUSIG	140	45000	120	1 micron std.cell

Specifications	
Formats	32 and 64 bit
No of registers	32 registers of 32 bits
Standard	Conforms to IEEE 754
Clock frequency	33 MHz
Linpack performance	0.75 MFLOPS

Features

- * General purpose bus interface
- * Provides 32 general purpose single precision registers or 16 double precision registers
- * 31-bit control and status registers
- * 64-bit internal architecture

☐ MMAC



MMAC is a multichannel multiplier accumulator designed for signal processing applications. It can be programmed for functions like (i) multichannel multiply accumulation/subtraction up to 48 bits, (ii) first and second order infinite impulse response (IIR) filters, and (iii) higher order filters by cascading through internal feedback path.

Features

- * Operating frequency 20 MHz
- * Supports up to 132 channels (user programmable)
- * Selectable 16 bit 2's complement or unsigned magnitude inputs
- * Standard TTL (transistor-transistor logic) compatible inputs and outputs
- * User-selectable mode of operation
- * Optional saturation, scaling and rounding facility for output

Since MMAC ASIC supports multichannel operations, it can be used in array signal processing applications, either in front-end filter circuit or in back-end signal processor circuit.

☐ FMAC

FMAC (fast multiplier and accumulator circuit), is a generic chip useful for many digital signal processing applications. It is basically a multiplier and an accumulator.

Features

- * It accepts unsigned/2's complement inputs
- * Operates in three modes, namely, multiply and accumulate, multiply, multiply and subtract

- * Internally synchronous reset
- * 5-stage pipelined architecture

Specifications

- * Inputs 16-bit
- * Accumulated output 36-bit
- * Clock rate 50 MHz
- * Independent enables for outputs
- * Separate clocks for inputs

□ Inverse Pythagora's Processor

This ASIC converts polar coordinates to cartesian co-ordinates. The chip accepts 16-bit magnitude and 16-bit phase inputs. The inputs can be given in 2's complement or sign magnitude formats. The co-ordinates conversion is done using the CORDIC algorithm. The algorithm is implemented with 26 stages of pipelining.

Specifications

- * Sine/cosine look up mode
- * 16-bit real and imaginary outputs
- * 20 MHz operating frequency

□ CMUL

CMUL (Complex Multiplier) basically multiplies two complex numbers and gives the complex product as output. It operates in two modes. In complex multiplier mode, it multiplies two complex words (16-bit each) every 50 nano seconds. In the filter mode, it adds 16 most significant bits of the multiplier result with input complex word.

Specifications

- * 2's complement fractional arithmetic
- * Trap logic for -1 into -1
- * Complex conjunction of either inputs
- * 20 MHz clock rate
- * Four cycle fall through

□ ANUSIG

ANUSIG (ANURAG's Digital Signal Processor) is a general purpose digital signal processor.

Features

- * Modified Harvard architecture
- * 16-bit integer and fixed point data format representation
- * 16K address space (program, data)
- * 40-bit accumulator width
- * Multi-function instructions
- * Four external interrupts
- * 12 MHz operating frequency

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